الفرقة الثالثة
٢٠١٦ / ١ / ٢١

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Electrical Engineering Dept. 3rd Year Jan. 2016
Computer Engineering 85 Marks

1. [10 M.]
(a).Comment :Computer- architecture , -organization , -design [2m]
(b).Draw block diagram Hard-Wired for: [8m]
(1)Single-Bus CPU structure (2) Two- Bus CPU structure
(3)Control Unit Organization (4)Implementing(3) with PLA

2. [16 M.]----------
Given an Instruction :
Stored in main memory as shown in Fig.(1)
(a) Write steps ,and control signals to Fetch and Execute Instruction
write the contents of(PC,MAR,Y,Z,MDR, [3Ch] in each steps [8m]
(b) Suggest suitable Partial Format for Field Encoded Microinstruction [8m]

3. [18 M.]----------
Given Flow-Chart of micro-program for the ADD instruction
ADD (Rsrc) + (Rdst) = Rdst
where Rsrc (register direct mode) ,while Rdst (register indirect mode)
(a)Write the control signals of micro-routine [6m]
(b)Suggest a suitable partial format of field-encoded micro-routine
Using Next-Address Field [6m]
(c)Implement (b) with bit-patterns [6m]

4. [14 M.]----------
(a).Draw Bipolar, N-MOS, Dynamic, and ROM Memory Cells ,and
Show how the Cell to be (1)Isolated (2) Read(H,L) (3) Write(H,L) [8m]
(b).Given 8 Chips Dynamic RAM, each 64Kx16
through block diagram show steps for (1)READ (2)Refreshments [6m]

5.[15 M]----------
(a)Show different modules for 32 Word RAM [6m]
(b)Given 32Kx16 main memory , show different mapping methods
with 1Kx16 Cache memory [9m]

من فضلك أنظر الصفحة الثانية

6. [12 M.]

(a) Explain briefly:

(1) CISC (2) RISC [6m]

(b) Given a 4 Instructions Program with 4 stages CPU [F,S,O,D] Show and Calculate total time using (i) CISC (ii) RISC ,and Calculate the speed-up factor in case of RISC [6m]

Fig.(1)

:	:
:	:
2F	Add [[3Ah]]+[[3Bh]] = [3Ch]
:	:
:	:
3A	4h
:	:
3B	6h
:	:
3C	
:	:
:	:
:	: